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Software Serial Port Implemented with the PCA

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For microcontroller applications which require more than one serial port, the 83C51FA Programmable Counter Array (PCA) can implement additional half-duplex serial ports. If the on-chip UART is being used as an inter-processor link, the PCA can be used to interface the 83C51FA to additional asynchronous lines.

This application uses several different Compare/Capture modes available on the PCA to receive or transmit bytes of data. It is assumed the reader is familiar the PCA and ASM51. For more information on the PCA refer to the "Hardware Description of the 83C51FA" chapter in the Embedded Controller Handbook (Order No. 210918).

Introduction

The figure below shows the format of a standard 10-bit asynchronous frame: 1 start bit (0), 8 data bits, and 1 stop bit (1). The start bit is used to synchronize the receiver to the transmitter; at the leading edge of the start bit the receiver must set up its timing logic to sample the incoming line in the center of each bit. Following the start bit are eight data bits which are transmitted least significant bit first. The stop bit is set to the opposite state of the start bit to guarantee that the leading edge of the start bit will cause a transition on the line. It also provides a dead time on the line so that the receiver can maintain its synchronization.

Two of the Compare/Capture modes on the PCA are used in receiving and transmitting data bits. When receiving, the Negative-Edge Capture mode allows the PCA to detect the start bit. Then using the Software Timer mode, interrupts are generated to sample the incoming data bits. This same mode is used to clock out bits when transmitting.

This Application Note contains four sections of code:

- (1) List of variables
- (2) Initialization routine

- (3) Receive routine
- (4) Transmit routine.

A complete listing of the routines and the test loop which was used to verify their operation is found in the Appendix. A total of three half-duplex channels were run at 2400 Baud in the test program. The listings shown here are simplified to one channel (Channel 0).

Variables

Listing 1 shows the variables used in both the receive and transmit routines. Flags are defined to signify the status of the reception or transmission of a byte (e.g. RCV_START_BIT, TXM_START_BIT). RCV_BUF and TXM_BUF simulate the on-chip serial port SBUF as two separate buffer registers. The temporary registers, RCV_REG and TXM_REG, are used to save bits as they are received or transmitted. Finally, two counter registers keep track of how many bits have been received or transmitted.

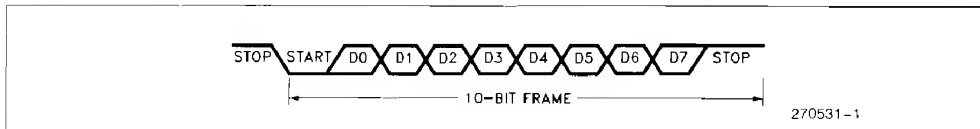
Variables are also needed to define one-half and one-full bit times in units of PCA timer ticks. (One bit time = $1 / \text{baud rate}$.) With the PCA timer incremented every machine cycle, the equation to calculate one bit time can be written as:

$$\frac{\text{Osc. Freq.}}{(12) \cdot (\text{baud rate})} = 1 \text{ bit time (in PCA timer ticks)}$$

In this example, the baud rate is 2400 at 16 MHz.

$$\frac{16 \text{ MHz}}{(12) \cdot (2400)} = 556 \text{ counts} = 22\text{C Hex}$$

The high and low byte of this value is placed in the variables FULL_BIT_HIGH and FULL_BIT_LOW, respectively. 115H is the value loaded into HALF_BIT_HIGH and HALF_BIT_LOW.



Listing 1. Variables used by the software serial port. Channel 0

```

;
; Receive Routine
;
RCV_START_BIT_0  BIT    20H.0    ; Indicates start bit
;                               ; has been received
RCV_DONE_0       BIT    20H.1    ; Indicates data byte
;                               ; has been received
RCV_BUF_0        DATA   30H      ; Software Receive
;                               ; "SBUF"
RCV_REG_0        DATA   31H      ; Temporary register
;                               ; for receive bits
RCV_COUNT_0      DATA   32H      ; Counter for receiving
;                               ; bits

; Transmit Routine:
;
TXM_START_BIT_0  BIT    20H.3    ; Indicates start bit
;                               ; has been transmitted
TXM_IN_PROGRESS_0 BIT    20H.4    ; Indicates transmit is
;                               ; in progress
TXM_BUF_0        DATA   34H      ; Software transmit
;                               ; "SBUF"
TXM_REG_0        DATA   35H      ; Temporary register
;                               ; for transmitting bits
TXM_COUNT_0      DATA   36H      ; Counter for transmit-
;                               ; ting bits
DATA_0          DATA   37H      ; Register used for the
;                               ; test program

;
NEG_EDGE         EQU     11H      ; Two modes of operation
S_W_TIMER        EQU     49H      ; for compare/capture
;                               ; modules

;
HALF_BIT_HIGH    EQU     01H      ; Half bit time = 115H
HALF_BIT_LOW     EQU     15H
FULL_BIT_HIGH    EQU     02H      ; Full bit time = 22CH
FULL_BIT_LOW     EQU     2CH      ; 2400 Baud at 16 MHz

```

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Initialization

Listing 2 contains the initialization code for the receive and transmit process. Module 0 of the PCA is used as a receiver and is first set up to detect a negative edge from the start bit. Modules 2 and 3 are used for the additional 2 channels (see the Appendix). Module 3 is used as a separate software timer to transmit bits.

Listing 2. Initialization Routine

```

ORG 0000H
LJMP INITIALIZE
ORG 001BH
LJMP RECEIVE_DONE          ; Timer 1 overflow -
                           ; simulates "RI" interrupt
ORG 0033H
LJMP RECEIVE              ; PCA interrupt
;
INITIALIZE: MOV SP, #5FH    ; Initialize stack pointer
                           ; (specific to test program)
INIT_PCA: MOV CMOD, #00H   ; Increment PCA timer
                           ; @ 1/12 Osc Frequency
                           ; Clear all status flags
                           ; Module 0 in negative-edge
                           ; trigger mode (Pl.3)
                           ; Module 3 as software timer
                           ; mode
                           MOV CCAPM0, #NEG_EDGE
                           MOV CCAPM3, #S_W_TIMER
                           MOV CL, #00H
                           MOV CH, #00H
                           MOV IE, #0D8H    ; Init all needed interrupts
                           ; EA, EC, ES, ET1
                           SETB CR          ; Turn on PCA Counter

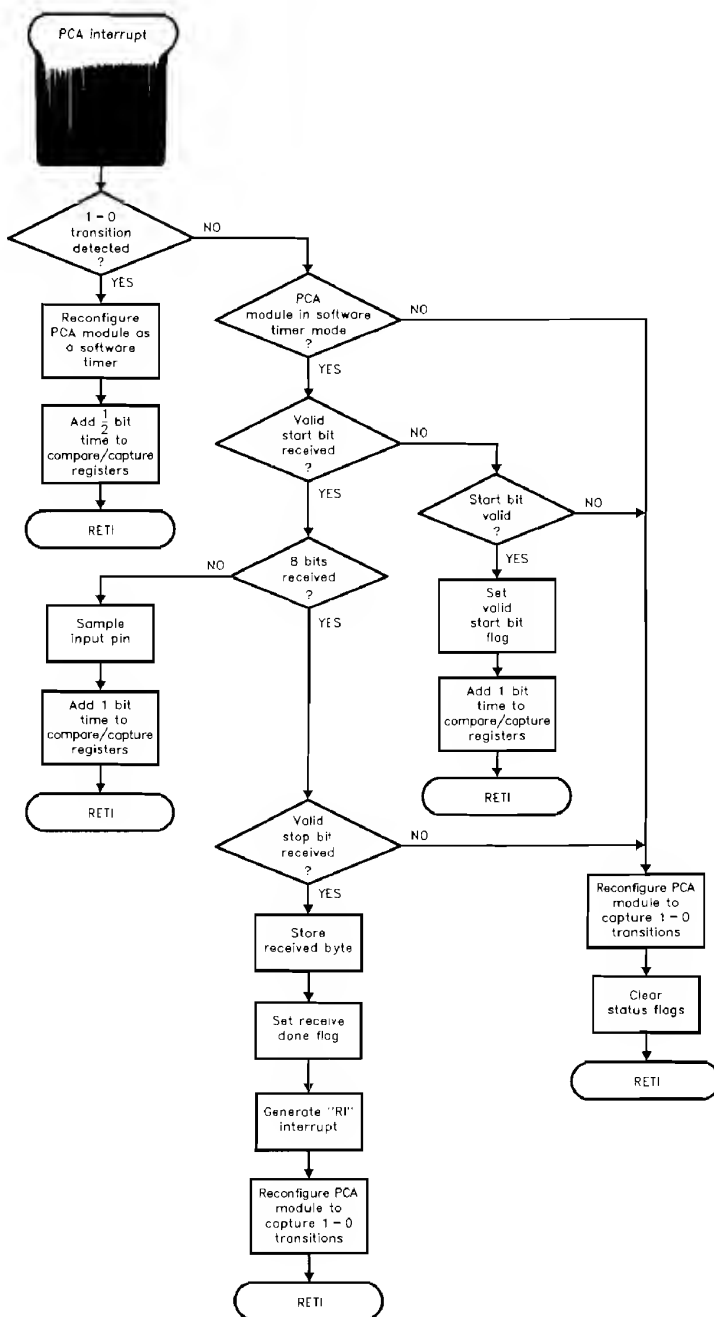
```

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All flags and registers from Listing 1 should be cleared in the initialization process.

Receive Routine

Two operating modes of the PCA are needed to receive bits. The module must first be able to detect the leading edge of a start bit so it is initially set up to capture a 1-to-0 transition (i.e. Negative-Edge Capture mode). The module is then reconfigured as a software timer to cause an interrupt at the center of each bit to deserialize the incoming data. The flowchart for the receive routine is given in Figure 1.



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Figure 1. Flowchart for the Receive Routine

Listing 3.1 shows the code needed to detect a start bit. Notice that the first software timer interrupt will occur one-half bit time after the leading edge of the start bit to check its validity. If it is valid, the RCV_START_BIT is set. The rest of the samples will occur a full bit time later. The RCV_COUNT register is loaded with a value of 9 which indicates the number of bits to be sampled: 8 data bits and 1 stop bit.

Listing 3.1. Receive Interrupt Routine

```

RECEIVE:  PUSH ACC
          PUSH PSW
;
MODULE_0: CLR CCF0           ; Assume reception on
          ; Module 0
          MOV A, CCAPM0       ; Check mode of module. If
          ANL A, #01111111B    ; set up to receive negative
          CJNE A, #NEG_EDGE, RCV_START_0 ; edges, then module
          ; is waiting for a start bit
;
          CLR C               ; Update compare/capture
          MOV A, #HALF_BIT_LOW ; registers for half bit time
          ADD A, CCAP0L        ; to sample start bit
          MOV CCAP0L, A        ; Half bit time = 115H
          MOV A, #HALF_BIT_HIGH
          ADDC A, CCAP0H
          MOV CCAP0H, A
          MOV CCAPM0, #S_W_TIMER ; Reconfigure module 0 as
          POP PSW              ; a software timer to sample
          POP ACC              ; bits
          RETI
;
RCV_START_0: CJNE A, #S_W_TIMER, ERROR_0 ; Check module is
          ; configured as a software
          ; timer, otherwise error.
          JB RCV_START_BIT_0, RCV_BYTE_0 ; Check if start bit
          ; is Received yet.
          JB P1.3, ERROR_0           ; Check that start bit = 0,
          ; otherwise error.
          SETB RCV_START_BIT_0       ; Signify valid start bit
          ; was received
          MOV RCV_COUNT_0, #09H      ; Start counting bits sampled
;
          CLR C                       ; Update compare/capture
          MOV A, #FULL_BIT_LOW        ; registers to sample
          ADD A, CCAP0L                ; incoming bits
          MOV CCAP0L, A                ; Full bit time = 22CH
          MOV A, #FULL_BIT_HIGH
          ADDC A, CCAP0H
          MOV CCAP0H, A
          POP PSW
          POP ACC
          RETI

```

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The next 8 timer interrupts will receive the incoming data bits; the RCV_COUNT register keeps track of how many bits have been sampled. As each bit is sampled, it is shifted through the Carry Flag and saved in RCV_REG. The ninth sample checks the validity of the stop bit. If it is valid, the data byte is moved into RCV_BUF.

The main routine must have a way to know that a byte has been received. With the on-chip UART, the RI (Receive Interrupt) bit is set whenever a byte has been received. For the software serial port, any unimplemented interrupt vector can be used to generate an interrupt when a byte has been received. This routine uses the Timer 1 Overflow interrupt (its selection is arbitrary). A routine to test this interrupt is included in the listing in the Appendix.

Listing 3.2. Receive Interrupt Routine (Continued)

```
RCV_BYTE_0: DJNZ RCV_COUNT_0, RCV_DATA_0 ; On 9th sample,
                                           ; check for valid stop bit
RCV_STOP_0: JNB P1.3, ERROR_0
             MOV RCV_BUF_0, RCV_REG_0 ; Save received byte in
                                           ; receive "SBUF"
             SETB RCV_DONE_0           ; Flag which module received
                                           ; a byte
             SETB TF1                  ; Generate an interrupt so
                                           ; main program knows a byte
                                           ; has been received
                                           ; (Note: selection of TF1 is
                                           ; arbitrary)
             MOV CCAPM0, #NEG_EDGE    ; Reconfigure module 0 for
                                           ; Reception of a start bit
             POP PSW
             POP ACC
             RETI

;
RCV_DATA_0: MOV C, P1.3                ; Sampling data bits
             MOV A, RCV_REG_0          ; Shifts bits thru CY into
             RRC A                     ; ACC
             MOV RCV_REG_0, A          ; Save each reception in
                                           ; temporary register
             CLR C                     ; Update c/c register for
             MOV A, #FULL_BIT_LOW      ; next sample time
             ADD A, CCAP0L
             MOV CCAP0L, A
             MOV A, #FULL_BIT_HIGH
             ADDC A, CCAP0H
             MOV CCAP0H, A
             POP PSW
             POP ACC
             RETI
```

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In addition, an error routine (Listing 3.3) is included for invalid start or stop bits to offer some protection against noise. If an error occurs, the module is re-initialized to look for another start bit.

Listing 3.3 Error Routine for Receive Routine

```
ERROR_0: MOV CCAPM0, #NEG_EDGE ; Reset module to look for
                                ; start bit
             CLR RCV_START_BIT_0 ; Clear flags which might
                                ; have been set
             POP PSW
             POP ACC
             RETI
```

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Transmit Routine

Another PCA module is configured as a software timer to interrupt the CPU every bit time. With each timer interrupt one or more bits can be transmitted through port pins. In the test program three channels were operated simultaneously, but in the listings below, one channel is shown for simplicity. The selection of port pins is user programmable. The flowchart for the transmit routine is given in Figure 2.

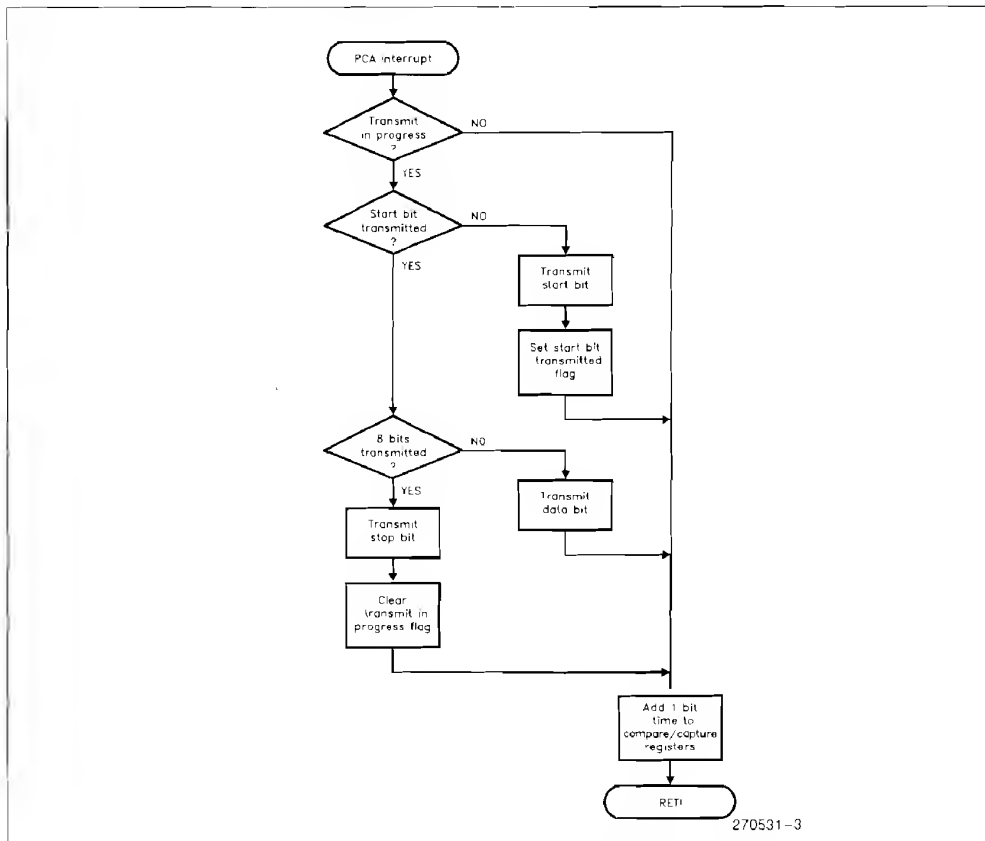


Figure 2. Flowchart for the Transmit Routine

When a byte is ready to be transmitted, the main program moves the data byte into the TXM_BUF register and sets the corresponding TXM_IN_PROGRESS bit. This bit informs the interrupt routine which channel is transmitting. The data byte is then moved in the storage register TXM_REG, and the TXM_COUNT is loaded. This main routine is shown in Listing 4.1.

Listing 4.1 Transmit Set Up Routine, Channel 0.

```

TXM_ON_0: CLR TXM_START_BIT_0    ; Clear status flag from
                                ; previous transmission
          MOV TXM_BUF_0, DATA_0 ; Load "SBUF" with data byte
          MOV TXM_REG_0, TXM_BUF_0
          MOV TXM_COUNT_0, #09    ; 8 data bits + 1 stop bit
          SETB TXM_IN_PROGRESS_0
    
```

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Listing 4.2 shows the transmit interrupt routine. The first time through, the start bit is transmitted. As each successive interrupt outputs a bit, the contents of TXM_REG is shifted right one place into the Carry flag, and the TXM_COUNT is decremented. When TXM_COUNT equals zero, the stop bit is transmitted.

Listing 4.2. Transmit Interrupt Routine

```

TRANSMIT: PUSH ACC
          PUSH PSW
          CLR CCF3                ; Clear s/w timer interrupt
                                   ; for transmitting bits
          JNB TXM_IN_PROGRESS_0, TRANSMIT_1 ; Check which
                                   ; channel is transmitting.
                                   ; "TRANSMIT_1" is listed in
                                   ; the Appendix
;
TRANSMIT_0: JB TXM_START_BIT_0, TXM_BYTE_0 ; If start bit
                                   ; has been sent, continue
                                   ; transmitting bits.
          CLR P3.2                ; Otherwise transmit start
                                   ; bit
          SETB TXM_START_BIT_0    ; Signify start bit sent
          JMP TXM_EXIT
;
TXM_BYTE_0: DJNZ TXM_COUNT_0, TXM_DATA_0 ; If bit count
                                   ; equals 1 thru 9, transmit
                                   ; data bits (8 total)
;
TXM_STOP_0: SETB P3.2            ; When bit count = 0,
                                   ; transmit stop bit
          CLR TXM_IN_PROGRESS_0 ; Indicate transmission is
                                   ; finished and ready for
                                   ; next byte
          JMP TXM_EXIT
;
TXM_DATA_0: MOV A, TXM_REG_0     ; Transmit one bit at a time
          RRC A                  ; through the carry bit
          MOV P3.2, C
          MOV TXM_REG_0, A       ; Save what's not been sent
;
TXM_EXIT: CLR C                  ; Update compare value with
          MOV A, #FULL_BIT_LOW  ; Full bit time = 22CH
          ADD A, CCAP3L
          MOV CCAP3L, A
          MOV A, #FULL_BIT_HIGH
          ADDC A, CCAP3H
          MOV CCAP3H, A
          POP PSW
          POP ACC
          RETI

```

270531-10

Conclusion

The software routines in the Appendix can be altered to vary the baud rate and number of channels to fit a particular application. The number of channels which can be implemented is limited by the CPU time required to service the PCA interrupt. At higher baud rates, fewer channels can be run.

The test program verifies the simultaneous operation of three half-duplex channels at 2400 Baud and the on-chip full-duplex channel at 9600 Baud. Thirty-three percent of the CPU time is required to operate all four channels. The test was run for several hours with no apparent malfunctions.

APPENDIX

01/01/80 PAGE 1

```

MCS-51 MACRO ASSEMBLER      SWPRT
DOS 3.20 (018-V) MCS-51 MACRO ASSEMBLER, V2.2
C:\PC\W018-V\BIN\MCS51.ASM
ASSEMBLER INVOKED BY: C:\MEDIA\ASM51.EXE SWPRT.RCV

LOC OBJ      LINE      SOURCE
1
2      SNOWDS1
3      SNCSWBOLS
4      SNOLIST
5
6      ; This program tests the receive routines of a software serial port.
7      ; Three half-duplex channels are implemented in software to run at:
8      ; 2400 baud (16Mhz). The on-chip serial port is also running full-duplex
9      ; at 9600 baud. Thirty-three percent of the CPU time is required to run
10     ; all four ports simultaneously.
11
12     ; To test the receive routines, "dummy" terminals transmit 00 - FF hex
13     ; continually to the PCA. When the first byte is received, it is
14     ; compared with 00. If the comparison is valid, the compare value is
15     ; incremented and the routine waits to receive the next byte. Error
16     ; routines toggle LEDs on port 2 to indicate an invalid comparison occurs
17     ; or if an invalid start bit or stop bit is received.
18
19     ORG 00H
20     LAMP INITIALIZE
21
22     ORG 0019H
23     LAMP RECEIVE_DONE
24
25     ORG 0023H
26     LAMP SERIAL_PORT
27
28     ORG 0033H
29     LAMP RECEIVE
30
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MC5-51 MACRO ASSEMBLER	SOURCE	LINE	LOC	OBJ
	RCV BUF_0	199	0030	
	RCV BUF_1	200	0040	
	RCV BUF_2	201	0050	
	RCV REG_0	202	0031	
	RCV REG_1	204	0041	
	RCV REG_2	205	0051	
	RCV COUNT_0	206	0032	
	RCV COUNT_1	207	0042	
	RCV COUNT_2	209	0052	
	COUNT_0	210		
	COUNT_1	211	0033	
	COUNT_2	212	0043	
	NEG_EDGE	214		
	S_W_THER	215	0011	
	HALF_BIT_LOW	216	0049	
	HALF_BIT_HIGH	218	0015	
	FULL_BIT_LOW	219	0001	
	FULL_BIT_HIGH	220	0002	
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	INITIALIZE:	229		
	INIT_PCA:	230		
	MOV SP, #5FH	231	0036 75815F	
	MOV CMO0, #00H	232	0039 75D900	
	MOV CC0N, #00H	233	003C 75D800	
	MOV CCAP40, #NEG_EDGE	234	003F 75DA11	
	MOV CCAP41, #NEG_EDGE	235	0042 75DB11	
	MOV CCAP42, #NEG_EDGE	236	0045 75DC11	
	MOV CL, #00H	237	0048 75E900	
	MOV CH, #00H	238	004B 75F000	
	MOV IE, #00BH	239	004E 75A8D8	
	SEIB CK	240	0051 D2DE	
	;	241		
	INIT_SP:	242		
	MOV SCON, #50H	243	0053 759850	
	MOV RCAP4H, #0FFH	244	0056 75CFFF	
	MOV RCAP2L, #0FCH	245	0059 75CACC	
	MOV TZCON, #3FH	246	005C 75C034	
	;	247		
	INIT_FLAGS:	248		
	CLR RCV_START_BIT_0	249	005F C200	
	CLR RCV_START_BIT_1	250	0061 C208	
	CLR RCV_START_BIT_2	251	0063 C210	
	CLR RCV_DONE_0	252	0065 C201	

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```

MCS-51 MACRO ASSEMBLER      SWPORT
LOC  OBJ      LINE      SOURCE
0067 C209      254      CLR RCV_DONE_1
0068 C211      255      CLR RCV_DONE_2
0069 C212      256      ;
006A C202      257      CLR RCV_ON_0
006B C203      258      CLR RCV_ON_1
006C C204      259      CLR RCV_ON_2
006D C212      260      ; Port 3 pins used in test program for error routines
006E C212      261      ;
006F C212      262      ;
0070 D282      263      ; Main program:
0071 D282      264      SETB P3.2
0072 D282      265      SETB P3.3
0073 D284      266      SETB P3.4
0074 D284      267      ;
0075 D285      268      ; Interrupt routines:
0076 D285      269      SETB P3.5
0077 D286      270      SETB P3.6
0078 D286      271      SETB P3.7
0079 D286      272      ;
007A D286      273      MOV RCV_BUF_0, #00H
007B D286      274      MOV RCV_BUF_1, #00H
007C D286      275      MOV RCV_BUF_2, #00H
007D D286      276      ;
007E D286      277      MOV RCV_COUNT_0, #00H
007F D286      278      MOV RCV_COUNT_1, #00H
0080 D286      279      MOV RCV_COUNT_2, #00H
0081 D286      280      ;
0082 D286      281      MOV RCV_REC_0, #00H
0083 D286      282      MOV RCV_REC_1, #00H
0084 D286      283      MOV RCV_REC_2, #00H
0085 D286      284      ;
0086 D286      285      MOV COUNT_0, #00H
0087 D286      286      MOV COUNT_1, #00H
0088 D286      287      MOV COUNT_2, #00H
0089 D286      288      ;
008A D286      289      ;
008B D286      290      ;
008C D286      291      ;
008D D286      292      ;
008E D286      293      ;
008F D286      294      ;
0090 D286      295      ;
0091 D286      296      ;
0092 D286      297      ;
0093 D286      298      ;
0094 D286      299      ;
0095 D286      300      ;
0096 D286      301      ;
0097 D286      302      ;
0098 D286      303      ;
0099 D286      304      ;
009A D286      305      ;
009B D286      306      ;
009C D286      307      ;
009D D286      308      ;

MAIN TEST ROUTINE - RECEIVE BITS
=====
CHECK_0:
JNB RCV_ON_0, CHECK_1
MOV A, RCV_BUF_0
CJNE A, COUNT_0, ERROR0
CLR RCV_ON_0
INC COUNT_0

CHECK_1:
JNB RCV_ON_1, CHECK_2
MOV A, RCV_BUF_1
CJNE A, COUNT_1, ERROR1
CLR RCV_ON_1
INC COUNT_1

CHECK_2:
JNB RCV_ON_2, CHECK_0
MOV A, RCV_BUF_2
CJNE A, COUNT_2, ERROR2

```

270531-13

PC	01/01/80	PC
SWPORT		
LOC	OBJ	LINE
00C1	2C12	309
00C3	0553	310
00C5	80DA	311
00C7	C2B2	312
00C9	75DA00	313
00CB	80DF	314
00CD	C2B3	315
00CF	7DB000	316
00D1	80E4	317
00D3	80E4	318
00D5	C2B4	319
00D7	75DA00	320
00D9	80E5	321
00DB	80E5	322
00DD	80E5	323
00DF	80E5	324
00E1	80E5	325
00E3	80E5	326
00E5	80E5	327
00E7	80E5	328
00E9	80E5	329
00EB	80E5	330
00ED	80E5	331
00EF	80E5	332
00F1	80E5	333
00F3	20D811	334
00F5	20D908	335
00F7	20DA08	336
00F9	20DB08	337
00FB	20DC08	338
00FD	80E5	339
00FF	80E5	340
0101	80E5	341
0103	80E5	342
0105	80E5	343
0107	80E5	344
0109	80E5	345
010B	80E5	346
010D	80E5	347
010F	80E5	348
0111	80E5	349
0113	80E5	350
0115	80E5	351
0117	80E5	352
0119	80E5	353
011B	80E5	354
011D	7415	355
011F	25FA	356
0121	25FA	357
0123	101A	358
0125	35FA	359
0127	35FA	360
0129	0108	361
012B	75DA49	362
012D	0109	363
012F	010F	364
0131	010F	365
0133	010F	366
0135	010F	367
0137	010F	368
0139	010F	369
013B	010F	370
013D	010F	371
013F	010F	372
0141	010F	373
0143	010F	374
0145	010F	375
0147	010F	376
0149	010F	377
014B	010F	378
014D	010F	379
014F	010F	380
0151	010F	381
0153	010F	382
0155	010F	383
0157	010F	384
0159	010F	385
015B	010F	386
015D	010F	387
015F	010F	388
0161	010F	389
0163	010F	390
0165	010F	391
0167	010F	392
0169	010F	393
016B	010F	394
016D	010F	395
016F	010F	396
0171	010F	397
0173	010F	398
0175	010F	399
0177	010F	400
0179	010F	401
017B	010F	402
017D	010F	403
017F	010F	404
0181	010F	405
0183	010F	406
0185	010F	407
0187	010F	408
0189	010F	409
018B	010F	410
018D	010F	411
018F	010F	412
0191	010F	413
0193	010F	414
0195	010F	415
0197	010F	416
0199	010F	417
019B	010F	418
019D	010F	419
019F	010F	420
01A1	010F	421
01A3	010F	422
01A5	010F	423
01A7	010F	424
01A9	010F	425
01AB	010F	426
01AD	010F	427
01AF	010F	428
01B1	010F	429
01B3	010F	430
01B5	010F	431
01B7	010F	432
01B9	010F	433
01BB	010F	434
01BD	010F	435
01BF	010F	436
01C1	010F	437
01C3	010F	438
01C5	010F	439
01C7	010F	440
01C9	010F	441
01CB	010F	442
01CD	010F	443
01CF	010F	444
01D1	010F	445
01D3	010F	446
01D5	010F	447
01D7	010F	448
01D9	010F	449
01DB	010F	450
01DD	010F	451
01DF	010F	452
01E1	010F	453
01E3	010F	454
01E5	010F	455
01E7	010F	456
01E9	010F	457
01EB	010F	458
01ED	010F	459
01EF	010F	460
01F1	010F	461
01F3	010F	462
01F5	010F	463
01F7	010F	464
01F9	010F	465
01FB	010F	466
01FD	010F	467
01FF	010F	468
0201	010F	469
0203	010F	470
0205	010F	471
0207	010F	472
0209	010F	473
020B	010F	474
020D	010F	475
020F	010F	476
0211	010F	477
0213	010F	478
0215	010F	479
0217	010F	480
0219	010F	481
021B	010F	482
021D	010F	483
021F	010F	484
0221	010F	485
0223	010F	486
0225	010F	487
0227	010F	488
0229	010F	489
022B	010F	490
022D	010F	491
022F	010F	492
0231	010F	493
0233	010F	494
0235	010F	495
0237	010F	496
0239	010F	497
023B	010F	498
023D	010F	499
023F	010F	500
0241	010F	501
0243	010F	502
0245	010F	503
0247	010F	504
0249	010F	505
024B	010F	506
024D	010F	507
024F	010F	508
0251	010F	509
0253	010F	510
0255	010F	511
0257	010F	512
0259	010F	513
025B	010F	514
025D	010F	515
025F	010F	516
0261	010F	517
0263	010F	518
0265	010F	519
0267	010F	520
0269	010F	521
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026F	010F	524
0271	010F	525
0273	010F	526
0275	010F	527
0277	010F	528
0279	010F	529
027B	010F	530
027D	010F	531
027F	010F	532
0281	010F	533
0283	010F	534
0285	010F	535
0287	010F	536
0289	010F	537
028B	010F	538
028D	010F	539
028F	010F	540
0291	010F	541
0293	010F	542
0295	010F	543
0297	010F	544
0299	010F	545
029B	010F	546
029D	010F	547
029F	010F	548
0301	010F	549
0303	010F	550
0305	010F	551
0307	010F	552
0309	010F	553
030B	010F	554
030D	010F	555
030F	010F	556
0311	010F	557
0313	010F	558
0315	010F	559
0317	010F	560
0319	010F	561
031B	010F	562
031D	010F	563
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0321	010F	565
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0325	010F	567
0327	010F	568
0329	010F	569
032B	010F	570
032D	010F	571
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0331	010F	573
0333	010F	574
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0337	010F	576
0339	010F	577
033B	010F	578
033D	010F	579
033F	010F	580
0341	010F	581
0343	010F	582
0345	010F	583
0347	010F	584
0349	010F	585
034B	010F	586
034D	010F	587
034F	010F	588
0351	010F	589
0353	010F	590
0355	010F	591
0357	010F	592
0359	010F	593
035B	010F	594
035D	010F	595
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0361	010F	597
0363	010F	598
0365	010F	599
0367	010F	600
0369	010F	601
036B	010F	602
036D	010F	603
036F	010F	604
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0373	010F	606
0375	010F	607
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037D	010F	611
037F	010F	612
0381	010F	613
0383	010F	614
0385	010F	615
0387	010F	616
0389	010F	617
038B	010F	618
038D	010F	619
038F	010F	620
0391	010F	621
0393	010F	622
0395	010F	623
0397	010F	624
0399	010F	625
039B	010F	626
039D	010F	627
039F	010F	628
0401	010F	629
0403	010F	630
0405	010F	631
0407	010F	632
0409	010F	633
040B	010F	634
040D	010F	635
040F	010F	636
0411	010F	637
0413	010F	638
0415	010F	639
0417	010F	640
0419	010F	641
041B	010F	642
041D	010F	643
041F	010F	644
0421	010F	645
0423	010F	646
0425	010F	647
0427	010F	648
0429	010F	649
042B	010F	650
042D	010F	651
042F	010F	652
0431	010F	653
0433	010F	654
0435	010F	655
0437	010F	656
0439	010F	657
043B	010F	658
043D	010F	659
043F	010F	660
0441	010F	661
0443	010F	662
0445	010F	663
0447	010F	664
0449	010F	665
044B	010F	666
044D	010F	667
044F	010F	668
0451	010F	669
0453	010F	670
0455	010F	671
0457	010F	672
0459	010F	673
045B	010F	674
045D	010F	675
045F	010F	676
0461	010F	677
0463	010F	678
0465	010F	679
0467	010F	680
0469	010F	681
046B	010F	682
046D	010F	683
046F	010F	684
0471	010F	685
0473	010F	686
0475	010F	687
0477	010F	688
0479	010F	689
047B	010F	690
047D	010F	691
047F	010F	692
0481	010F	693
0483	010F	694
0485	010F	695
0487	010F	696
0489	010F	697
048B	010F	698
048D	010F	699
048F	010F	700
0491	010F	701
0493	010F	702
0495	010F	703
0497	010F	704
0499	010F	705
049B	010F	706
049D	010F	707
049F	010F	708
0501	010F	709
0503	010F	710
0505	010F	711
0507	010F	712
0509	010F	713
050B	010F	714
050D	010F	715
050F	010F	716
0511	010F	717
0513	010F	718
0515	010F	719
0517		

MCS-51 MACRO ASSEMBLER SWF08T

LOC	OBJ	LINE	SOURCE
0111 32		364	RETI
0112 84494B		365	RCV_START_0: CNE A, #S_W_TIMER, ERROR_0
0115 20001A		366	JB RCV_START_BIT_0, RCV_BYTE_0
0118 209345		367	JB P1_3, ERROR_0
011B 0200		368	SETB RCV_START_BIT_0
011D 753209		369	MOV RCV_COUNT_0, #09H
0120 C3		370	CLR C
0121 742C		371	MOV A, #FULL_BIT_LOW
0122 555A		372	MOV C, CCF0H
0123 742C		373	MOV A, #FULL_BIT_HIGH
0124 555A		374	MOV C, CCF0H
0125 742C		375	ADD A, CCF0H
0126 555A		376	MOV C, CCF0H
0127 555A		377	POP PSW
0128 0060		378	POP ACC
0129 0060		379	RETI
0130 0060		380	
0131 3260		381	
0132 D53212		382	RCV_BYTE_0: DJNZ RCV_COUNT_0, RCV_DATA_0
0135 209338		383	JNB P1_3, ERROR_0
0136 853130		384	MOV RCV_BUF_0, RCV_REG_0
0138 0201		385	SETB RCV_DONE_0
013D 028F		386	SETB T1
013F 75D811		387	MOV C, #NEG_EDGE
0142 0060		388	POP PSW
0144 0060		389	POP ACC
0146 32		390	RETI
0147 4283		391	RCV_DATA_0: MOV C, P1_3
0149 853131		392	MOV A, RCV_REG_0
014B 13		393	RRC A
014C 6531		394	MOV RCV_REG_0, A
014E C32C		395	CLR C
0150 752A		396	MOV A, #FULL_BIT_LOW
0151 555A		397	MOV C, CCF0H
0153 555A		398	ADD A, CCF0H
0155 7402		399	MOV A, #FULL_BIT_HIGH
0157 355A		400	ADD A, CCF0H
0159 555A		401	MOV C, CCF0H
015B 0060		402	POP PSW
015D 0060		403	POP ACC
015F 32		404	RETI
0160 C285		405	ERROR_0: CLR P3_5
		406	
		407	

MCS-51 MACRO ASSEMBLER SWPOT

LOC	OBJ	LINE	SOURCE
418			
0162	75D411	419	MOV CCAPM0, INEG_EDGE
0165	C200	420	CLR RCV_START_BIT_0
0167	D0D0	421	POP PSW
0169	D0E0	422	POP ACC
016B	32	423	RETI
424			
425			
426			
427			
428			
016C	C209	429	CLR CCF1
016E	75D411	430	MOV CCAPM1, INEG_EDGE
0170	547F	431	ANL A, #01111111B
0172	B41115	432	CJNE A, INEG_EDGE, RCV_START_1
433			
0175	C3	434	CLR C
0176	75D411	435	MOV CCAP1, HALF_BIT_LOW
0178	25EB	436	ADD A, CCAP1
017A	F5EB	437	MOV CCAP1, A
017C	7401	438	MOV A, HALF_BIT_HIGH
017E	35FB	439	ADD A, CCAP1
0180	75D411	440	MOV CCAP1, A
0182	75D411	441	MOV CCAPM1, PS_TIMER
0185	D0D0	442	POP PSW
0187	D0E0	443	POP ACC
0189	32	444	RETI
445			
018A	B484B	446	CJNE A, IS_M_TIMER, ERROR_1
018C	2081A	447	JB RCV_START_BIT_1, RCV_BYTE_1
0190	209445	448	JB PL_4, ERROR_1
449			
0193	D208	450	SETB RCV_START_BIT_1
0195	754209	451	MOV RCV_COUNT_1, #09H
453			
0198	C3	453	CLR C
0199	742C	454	MOV A, #FULL_BIT_LOW
019B	25EB	455	ADD A, CCAP1
019D	75D411	456	MOV CCAP1, A
019F	75D411	457	MOV A, #FULL_BIT_HIGH
01A1	35FB	458	ADD A, CCAP1
01A3	F5FB	459	MOV CCAP1, A
01A5	D0D0	460	POP PSW
01A7	D0E0	461	POP ACC
01A9	32	462	RETI
463			
01AA	D54212	464	DJNZ RCV_COUNT_1, RCV_DATA_1
465			
01AD	309428	466	JNB PL_4, ERROR_1
01B0	854140	467	MOV RCV_BUF_1, RCV_REG_1
01B3	D28F	468	SETB RCV_DONE_1
01B7	75D411	469	MOV CCAPM1, INEG_EDGE
01BA	D0D0	470	POP PSW
01BC	D0E0	471	POP ACC
472			

MCS-51 MACRO ASSEMBLER SMPRT

LOC OBJ LINE SOURCE

```

473 RETI
474 MOV C, P1.4
475 MOV A, RCV_REG_1
476 RRC A,
477 MOV RCV_REG_1, A
478
479 CLR C
480 CLR A, FULL_BIT_LOW
481 ADD A, CCAP1L
482 MOV A, CCAP1L
483 MOV A, CCAP1L
484 MOV A, FULL_BIT_HIGH
485 ADDC A, CCAP1H
486 MOV A, CCAP1H
487 POP PSW
488 POP ACC
489 RETI
490
491 CLR F3.6
492 CLR F3.6H, INEG_EDGE
493 CLR RCV_START_BIT_1
494 POP PSW
495 POP ACC
496 RETI
497
498 ;
499 ;
500 ;
501 ;
502 ;
503 ;
504 MODULE_2:
505
506 CLR CCF2
507 MOV A, CCAPM2
508 ANL A, #01111111B
509 CINE A, INEG_EDGE, RCV_START_2
510
511 CLR C
512 MOV A, HALF_BIT_LOW
513 ADD A, CCAP2L
514 MOV A, CCAP2L
515 MOV A, HALF_BIT_HIGH
516 ADDC A, CCAP2H
517 MOV A, CCAP2H
518 MOV A, CCAP2H
519 POP PSW
520 POP ACC
521 RETI
522
523 RCV_START_2:
524 JB RCV_START_BIT_2, RCV_BYTE_2
525 JB P1.5, ERROR_2
526
527 SETB RCV_START_BIT_2
528 MOV RCV_COUNT_2, #05H
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```

CHANNEL 2

; Similar to module 0

MCS-51 MACRO ASSEMBLER

SNMPT

LOC OBJ LINE SOURCE

```

508 CLR C, IFULL_BIT_LOW
509 MOV A, CCAP2L, A
510 ADD A, CCAP2L, A
511 MOV CCAP2L, A
512 MOV A, IFULL_BIT_HIGH
513 ADD A, CCAP2H, A
514 MOV CCAP2H, A
515 POP PSW
516 POP ACC
517 RETI

```

```

518 ; RCV_BYTE_2:
519 JNZ RCV_COUNT_2, RCV_DATA_2

```

```

520 ; RCV_STOP_2:
521 MOV RCV_AUF_2, RCV_REG_2
522 SETB RCV_DONE_2, RCV_REG_2
523 SETB TFI_
524 MOV CCAPM2, INEG_EDGE
525 POP PSW
526 POP ACC
527 RETI

```

```

528 ; RCV_DATA_2:

```

```

529 MOV C, PL5
530 MOV A, RCV_REG_2
531 INC A
532 MOV RCV_REG_2, A
533 CLR C
534 MOV A, IFULL_BIT_LOW
535 ADD A, CCAP2L
536 MOV CCAP2L, A
537 MOV A, IFULL_BIT_HIGH
538 ADD A, CCAP2H, A
539 MOV CCAP2H, A
540 POP PSW
541 POP ACC
542 RETI

```

```

543 ; ERROR_2:

```

```

544 CLR P3.7
545 MOV CCAPM2, INEG_EDGE
546 CLR RCV_START_BIT_2
547 POP PSW
548 POP ACC
549 RETI

```

```

550 ;
551 ; This routine simulates the "RI" interrupt. When a byte is received on one
552 ; of the channels, this interrupt is generated. Bits are set so the main
553 ; routine knows which channel received a byte.
554 ;

```

```

555 ; RECEIVE_DONE:

```

```

556 PUSH ACC
557 PUSH PSW
558 CLR TFI
559
560
561
562
563
564

```

```

025C C0E0
025E C0D0
0260 C28F

```

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MCS-51 MACRO ASSEMBLER

SNPORT

LOC OBJ LINE SOURCE

```

0262 300106 583 JNB RCV_DONE_0, RCV_1 ; Check which module received a byte
0263 C201 584 CLR RCV_DONE_0 ; Clear flags needed for next reception
0264 C200 585 SETB RCV_ON_0 ; Tell main routine which channel received
0265 D202 586 ; a byte

```

RCV_1:

```

0266 300906 588 JNB RCV_DONE_1, RCV_2
0267 C209 589 CLR RCV_DONE_1
0268 C208 590 SETB RCV_ON_1
0269 D20A 591 ;

```

RCV_2:

```

0274 301106 593 JNB RCV_DONE_2, RETURN
0275 C211 594 CLR RCV_DONE_2
0276 C210 595 SETB RCV_ON_2
0277 D212 596 ;

```

RETURN:

```

027D D0D0 598 POP PSW
027E D0E0 599 POP ACC
0281 32 600 RETI

```

SERIAL_PORT_INTERRUPT

```

; When a byte is received on the full-duplex serial port, it is then
; transmitted back to a "dummy" terminal. This terminal checks that the
; byte it transmitted to the PCA is the same value it receives back.

```

SERIAL_PORT:

```

0282 C0E0 602 PUSH ACC
0283 C0D0 603 PUSH PSW
0284 C0D0 604 JNB RI, TXM ; Check whether RI or TI
0285 30980B 605 MOV A, SEUF ; caused the interrupt
0286 E599 606 CLR RI, SEUF
0287 C298 607 JNB SEUF, A
0288 D0D3 608 POP PSW
0289 D0D3 609 POP ACC
0290 D0E0 610 RETI
0291 D0E0 611 ;
0292 32 612 ;

```

TXM:

```

0294 C099 622 CLR TI
0295 C0E0 623 POP PSW
0296 D0E0 624 POP ACC
029A 32 625 RETI
029B 32 626 ;
029C 32 627 ;
029D 32 628 ; END

```

REGISTER BANK(S) USED: 0

ASSEMBLY COMPLETE, NO ERRORS FOUND

270531-19

01/01/80 PAGE: 1

MCS-51 MACRO ASSEMBLER SWPORT
 DOS 1.20 (018-N) MCS-51 MACRO ASSEMBLER, V2.2
 OBJECT MODULE PLACED IN SWPORT.OBJ
 ASSEMBLER INVOKED BY: C:\EDIT\ASM51.EXE SWPORT.TR

LOC	OBJ	LINE	SOURCE
		1	\$NOMOD51
		2	\$NOSYMBOLS
		3	\$NOLIST
		152	;
		153	;
		154	;
		155	;
		156	;
		157	;
		158	;
		159	;
		160	;
		161	;
		162	;
		163	;
		164	ORG 00H
		165	LMP INIT_TXM
		166	;
		167	ORG 0023H
		168	LMP SERIAL_PORT
		169	;
		170	ORG 0033H
		171	LMP TRANSMIT
		172	;
		173	;
		174	;
		175	;
		176	;
		177	TXM START_BIT_0
		178	TXM START_BIT_1
		179	TXM START_BIT_2
		180	;
		181	TXM IN_PROGRESS_0
		182	TXM IN_PROGRESS_1
		183	TXM IN_PROGRESS_2
		184	;
		185	TXM BUF_0
		186	TXM BUF_1
		187	TXM BUF_2
		188	;
		189	TXM REG_0
		190	TXM REG_1
		191	TXM REG_2
		192	;
		193	TXM COUNT_0
		194	TXM COUNT_1
		195	TXM COUNT_2
		196	;
		197	DATA_0
		198	DATA_1
0000	020036		
0023	020148		
0033	0200D0		

; This program tests the transmit routines for the software serial port.
 ; To initialize the first transmission, the compare values are loaded before
 ; the PCA timer is started. Successive interrupts are generated every bit
 ; time by the software timer.
 ; For test purposes, the data transmitted increments from 00 to FF hex.
 ; "Dummy" terminals receive these bytes and display the bytes as they
 ; are incremented.
 ; Serial port interrupt
 ; PCA software timer interrupt
 ; Software transmit *SBUF*
 ; Temporary register for
 ; transmitting bits
 ; Counter for transmitting bits
 ; Register used for the test
 ; program

270651-20

LOC	OBJ	LINE	SOURCE	DATA	5/H
0057		199	DATA_2		
0049		200	5_W_TIMER	EQU	49H
002C		202	FULL_BIT_LOW	EQU	2CH
0002		204	FULL_BIT_HIGH	EQU	02H
		205			
		206			
		207			
		208	INITIALIZATION		
		209			
0036 75815F		210	INIT_TXM:	MOV SP, #5FH	
0439 759800		212		MOV CCON, #00H	
043C 759800		213		MOV CH, #00H	
043F 759800		214		MOV CL, #00H	
0442 759800		215		MOV CCAPM3, #5_W_TIMER	
0445 75D049		216			
		217			
0048 75A808		218		MOV IE, #0D9H	
		219			
004B 759850		220	INIT_SP:	MOV SCON, #50H	
004E 75C8FF		221		MOV RCAP2H, #0FFH	
0051 75C8C0		222		MOV RCAP2L, #00CH	
0054 75C834		223		MOV TICON, #34H	
		224			
		225	INIT_FLAGS:	CLR TXM_START_BIT_0	
0057 C203		226		CLR TXM_START_BIT_1	
0059 C208		227		CLR TXM_START_BIT_2	
005B C213		228			
		229			
005D C204		230		CLR TXM_IN_PROGRESS_0	
005F C20C		231		CLR TXM_IN_PROGRESS_1	
0061 C214		232		CLR TXM_IN_PROGRESS_2	
		233			
0063 753400		234		MOV TXM_BUF_0, #00H	
0066 754400		235		MOV TXM_BUF_1, #00H	
0069 755400		236		MOV TXM_BUF_2, #00H	
		237			
006C 753500		238		MOV TXM_REG_0, #00H	
006F 754500		239		MOV TXM_REG_1, #00H	
0072 755500		240		MOV TXM_REG_2, #00H	
		241			
0075 753600		242		MOV TXM_COUNT_0, #00H	
0078 754600		243		MOV TXM_COUNT_1, #00H	
007B 755600		244		MOV TXM_COUNT_2, #00H	
		245			
007E 7537FF		246		MOV DATA_0, #0FFH	
0081 7547FF		247		MOV DATA_1, #0FFH	
0084 7557FF		248		MOV DATA_2, #0FFH	
		249			
0087 75590C		250		MOV CCAP3L, #2CH	
008A 75D002		251		MOV CCAP3H, #02H	
008D 020E		252		SETB CR	
		253			

MCS-51 MACRO ASSEMBLER SWPORT

LOC	OBJ	LINE	SOURCE
254			MAIN TEST ROUTINE - TRANSMIT BITS
255			=====
256			
257			
258			FIRST_TXM:
259			JMP TXM_ON_0
260			MAIN_TXM:
261			JNB TXM_IN_PROGRESS_0, TXM_ON_0 ; Determine if ready to send
262			JNB TXM_IN_PROGRESS_1, TXM_ON_1 ; next byte. (i.e. transmit
263			JNB TXM_IN_PROGRESS_2, TXM_ON_2 ; not in progress)
264			JMP MAIN_TXM ; Waiting for '1' flag
265			
266			CLR TXM_START_BIT_0 ; Clear flag from previous
267			INC DATA_BUF_0, DATA_0 ; transmission
268			MOV TXM_REG_0, TXM_BUF_0 ; Load '800H' with data byte
269			MOV TXM_COUNT_0, #D9H ; 8 data bits + 1 stop bit
270			SETB TXM_IN_PROGRESS_0
271			JMP MAIN_TXM
272			
273			TXM_ON_1:
274			CLR TXM_START_BIT_1
275			INC DATA_1
276			MOV TXM_BUF_1, DATA_1
277			MOV TXM_REG_1, TXM_BUF_1
278			MOV TXM_COUNT_1, #D9H
279			SETB TXM_IN_PROGRESS_1
280			JMP MAIN_TXM
281			
282			TXM_ON_2:
283			CLR TXM_START_BIT_2
284			INC DATA_2
285			MOV TXM_BUF_2, DATA_2
286			MOV TXM_REG_2, TXM_BUF_2
287			MOV TXM_COUNT_2, #D9H
288			SETB TXM_IN_PROGRESS_2
289			JMP MAIN_TXM
290			
291			PCA_INTERRUPT_ROUTINE - TRANSMIT BITS
292			=====
293			
294			PUSH ACC
295			PUSH PCW
296			CLR CCF3
297			JNB TXM_IN_PROGRESS_0, TRANSMIT_1 ; Clear s/w timer interrupt
298			; Check which channel is
299			; transmitting
300			CHANNEL_0
301			=====
302			TRANSMIT_0:
303			JB TXM_START_BIT_0, TXM_BYTE_0 ; If start bit has been sent,
304			; continue transmitting data bits,
305			CLR PJ_2 ; otherwise transmit start bit
306			SETB TXM_START_BIT_0 ; Start next transmission
307			JMP TRANSMIT_1
308			; Check next transmit pin
0000	C0E0		
0001	C0E1		
0002	C0D8		
0006	30041E		
0009	200307		
000C	C2B2		
000E	D033		
0010	D033		
0010	0200F7		

MCS-51 MACRO

```

LOC      LOC      SOURCE
OBJ
LINE
309      TXM_BYTE_0:      DJNZ TXM_COUNT_0, TXM_DATA_0
310
311      TXM_STOP_0:      SETB P3.2
312      CLR TXM_IN_PROGRESS_0
313
314      JMP TXM_TRANSMIT_1
315
316      TXM_DATA_0:      MOV A, TXM_REG_0
317      RRC A
318      RRC P3.2, C
319      MOV TXM_REG_0, A
320      JMP TXM_TRANSMIT_1
321
322      ;
323      ;
324      ;
325      TXM_TRANSMIT_1:      JNB TXM_IN_PROGRESS_1, TXM_TRANSMIT_2 ; Similar to TXM_TRANSMIT_0
326      JB TXM_START_BIT_1, TXM_BYTE_1
327      CLR P3.3
328      SETB TXM_START_BIT_1
329      JMP TXM_TRANSMIT_2
330
331      TXM_BYTE_1:      DJNZ TXM_COUNT_1, TXM_DATA_1
332
333      TXM_STOP_1:      SETB P3.3
334      CLR TXM_IN_PROGRESS_1
335      JMP TXM_TRANSMIT_2
336
337      TXM_DATA_1:      MOV A, TXM_REG_1
338      RRC A
339      RRC P3.3, C
340      MOV TXM_REG_1, A
341      JMP TXM_TRANSMIT_2
342
343      ;
344      ;
345      ;
346      TXM_TRANSMIT_2:      JNB TXM_IN_PROGRESS_2, TXM_EXIT ; Similar to TXM_TRANSMIT_0
347      JB TXM_START_BIT_2, TXM_BYTE_2
348      CLR P3.4
349      SETB TXM_START_BIT_2
350      JMP TXM_EXIT
351
352      TXM_BYTE_2:      DJNZ TXM_COUNT_2, TXM_DATA_2
353
354      TXM_STOP_2:      SETB P3.4
355      CLR TXM_IN_PROGRESS_2
356      JMP TXM_EXIT
357
358      TXM_DATA_2:      MOV A, TXM_REG_2
359      RRC A
360      RRC P3.4, C
361      MOV TXM_REG_2, A
362      JMP TXM_EXIT
363
364      ;
365      ;
366      ;
367      TXM_TRANSMIT_3:      JNB TXM_IN_PROGRESS_3, TXM_TRANSMIT_4 ; Similar to TXM_TRANSMIT_0
368      JB TXM_START_BIT_3, TXM_BYTE_3
369      CLR P3.5
370      SETB TXM_START_BIT_3
371      JMP TXM_TRANSMIT_4
372
373      TXM_BYTE_3:      DJNZ TXM_COUNT_3, TXM_DATA_3
374
375      TXM_STOP_3:      SETB P3.5
376      CLR TXM_IN_PROGRESS_3
377      JMP TXM_TRANSMIT_4
378
379      TXM_DATA_3:      MOV A, TXM_REG_3
380      RRC A
381      RRC P3.5, C
382      MOV TXM_REG_3, A
383      JMP TXM_TRANSMIT_4
384
385      ;
386      ;
387      ;
388      TXM_TRANSMIT_4:      JNB TXM_IN_PROGRESS_4, TXM_TRANSMIT_5 ; Similar to TXM_TRANSMIT_0
389      JB TXM_START_BIT_4, TXM_BYTE_4
390      CLR P3.6
391      SETB TXM_START_BIT_4
392      JMP TXM_TRANSMIT_5
393
394      TXM_BYTE_4:      DJNZ TXM_COUNT_4, TXM_DATA_4
395
396      TXM_STOP_4:      SETB P3.6
397      CLR TXM_IN_PROGRESS_4
398      JMP TXM_EXIT
399
400      TXM_DATA_4:      MOV A, TXM_REG_4
401      RRC A
402      RRC P3.6, C
403      MOV TXM_REG_4, A
404      JMP TXM_EXIT
405
406      ;
407      ;
408      ;
409      TXM_TRANSMIT_5:      JNB TXM_IN_PROGRESS_5, TXM_TRANSMIT_6 ; Similar to TXM_TRANSMIT_0
410      JB TXM_START_BIT_5, TXM_BYTE_5
411      CLR P3.7
412      SETB TXM_START_BIT_5
413      JMP TXM_TRANSMIT_6
414
415      TXM_BYTE_5:      DJNZ TXM_COUNT_5, TXM_DATA_5
416
417      TXM_STOP_5:      SETB P3.7
418      CLR TXM_IN_PROGRESS_5
419      JMP TXM_EXIT
420
421      TXM_DATA_5:      MOV A, TXM_REG_5
422      RRC A
423      RRC P3.7, C
424      MOV TXM_REG_5, A
425      JMP TXM_EXIT
426
427      ;
428      ;
429      ;
430      TXM_TRANSMIT_6:      JNB TXM_IN_PROGRESS_6, TXM_TRANSMIT_7 ; Similar to TXM_TRANSMIT_0
431      JB TXM_START_BIT_6, TXM_BYTE_6
432      CLR P3.7
433      SETB TXM_START_BIT_6
434      JMP TXM_TRANSMIT_7
435
436      TXM_BYTE_6:      DJNZ TXM_COUNT_6, TXM_DATA_6
437
438      TXM_STOP_6:      SETB P3.7
439      CLR TXM_IN_PROGRESS_6
440      JMP TXM_EXIT
441
442      TXM_DATA_6:      MOV A, TXM_REG_6
443      RRC A
444      RRC P3.7, C
445      MOV TXM_REG_6, A
446      JMP TXM_EXIT
447
448      ;
449      ;
450      ;
451      TXM_TRANSMIT_7:      JNB TXM_IN_PROGRESS_7, TXM_TRANSMIT_8 ; Similar to TXM_TRANSMIT_0
452      JB TXM_START_BIT_7, TXM_BYTE_7
453      CLR P3.7
454      SETB TXM_START_BIT_7
455      JMP TXM_TRANSMIT_8
456
457      TXM_BYTE_7:      DJNZ TXM_COUNT_7, TXM_DATA_7
458
459      TXM_STOP_7:      SETB P3.7
460      CLR TXM_IN_PROGRESS_7
461      JMP TXM_EXIT
462
463      TXM_DATA_7:      MOV A, TXM_REG_7
464      RRC A
465      RRC P3.7, C
466      MOV TXM_REG_7, A
467      JMP TXM_EXIT
468
469      ;
470      ;
471      ;
472      TXM_TRANSMIT_8:      JNB TXM_IN_PROGRESS_8, TXM_TRANSMIT_9 ; Similar to TXM_TRANSMIT_0
473      JB TXM_START_BIT_8, TXM_BYTE_8
474      CLR P3.7
475      SETB TXM_START_BIT_8
476      JMP TXM_TRANSMIT_9
477
478      TXM_BYTE_8:      DJNZ TXM_COUNT_8, TXM_DATA_8
479
480      TXM_STOP_8:      SETB P3.7
481      CLR TXM_IN_PROGRESS_8
482      JMP TXM_EXIT
483
484      TXM_DATA_8:      MOV A, TXM_REG_8
485      RRC A
486      RRC P3.7, C
487      MOV TXM_REG_8, A
488      JMP TXM_EXIT
489
490      ;
491      ;
492      ;
493      TXM_TRANSMIT_9:      JNB TXM_IN_PROGRESS_9, TXM_TRANSMIT_10 ; Similar to TXM_TRANSMIT_0
494      JB TXM_START_BIT_9, TXM_BYTE_9
495      CLR P3.7
496      SETB TXM_START_BIT_9
497      JMP TXM_TRANSMIT_10
498
499      TXM_BYTE_9:      DJNZ TXM_COUNT_9, TXM_DATA_9
500
501      TXM_STOP_9:      SETB P3.7
502      CLR TXM_IN_PROGRESS_9
503      JMP TXM_EXIT
504
505      TXM_DATA_9:      MOV A, TXM_REG_9
506      RRC A
507      RRC P3.7, C
508      MOV TXM_REG_9, A
509      JMP TXM_EXIT
510
511      ;
512      ;
513      ;
514      TXM_TRANSMIT_10:      JNB TXM_IN_PROGRESS_10, TXM_TRANSMIT_11 ; Similar to TXM_TRANSMIT_0
515      JB TXM_START_BIT_10, TXM_BYTE_10
516      CLR P3.7
517      SETB TXM_START_BIT_10
518      JMP TXM_TRANSMIT_11
519
520      TXM_BYTE_10:      DJNZ TXM_COUNT_10, TXM_DATA_10
521
522      TXM_STOP_10:      SETB P3.7
523      CLR TXM_IN_PROGRESS_10
524      JMP TXM_EXIT
525
526      TXM_DATA_10:      MOV A, TXM_REG_10
527      RRC A
528      RRC P3.7, C
529      MOV TXM_REG_10, A
530      JMP TXM_EXIT
531
532      ;
533      ;
534      ;
535      TXM_TRANSMIT_11:      JNB TXM_IN_PROGRESS_11, TXM_TRANSMIT_12 ; Similar to TXM_TRANSMIT_0
536      JB TXM_START_BIT_11, TXM_BYTE_11
537      CLR P3.7
538      SETB TXM_START_BIT_11
539      JMP TXM_TRANSMIT_12
540
541      TXM_BYTE_11:      DJNZ TXM_COUNT_11, TXM_DATA_11
542
543      TXM_STOP_11:      SETB P3.7
544      CLR TXM_IN_PROGRESS_11
545      JMP TXM_EXIT
546
547      TXM_DATA_11:      MOV A, TXM_REG_11
548      RRC A
549      RRC P3.7, C
550      MOV TXM_REG_11, A
551      JMP TXM_EXIT
552
553      ;
554      ;
555      ;
556      TXM_TRANSMIT_12:      JNB TXM_IN_PROGRESS_12, TXM_TRANSMIT_13 ; Similar to TXM_TRANSMIT_0
557      JB TXM_START_BIT_12, TXM_BYTE_12
558      CLR P3.7
559      SETB TXM_START_BIT_12
560      JMP TXM_TRANSMIT_13
561
562      TXM_BYTE_12:      DJNZ TXM_COUNT_12, TXM_DATA_12
563
564      TXM_STOP_12:      SETB P3.7
565      CLR TXM_IN_PROGRESS_12
566      JMP TXM_EXIT
567
568      TXM_DATA_12:      MOV A, TXM_REG_12
569      RRC A
570      RRC P3.7, C
571      MOV TXM_REG_12, A
572      JMP TXM_EXIT
573
574      ;
575      ;
576      ;
577      TXM_TRANSMIT_13:      JNB TXM_IN_PROGRESS_13, TXM_TRANSMIT_14 ; Similar to TXM_TRANSMIT_0
578      JB TXM_START_BIT_13, TXM_BYTE_13
579      CLR P3.7
580      SETB TXM_START_BIT_13
581      JMP TXM_TRANSMIT_14
582
583      TXM_BYTE_13:      DJNZ TXM_COUNT_13, TXM_DATA_13
584
585      TXM_STOP_13:      SETB P3.7
586      CLR TXM_IN_PROGRESS_13
587      JMP TXM_EXIT
588
589      TXM_DATA_13:      MOV A, TXM_REG_13
590      RRC A
591      RRC P3.7, C
592      MOV TXM_REG_13, A
593      JMP TXM_EXIT
594
595      ;
596      ;
597      ;
598      TXM_TRANSMIT_14:      JNB TXM_IN_PROGRESS_14, TXM_TRANSMIT_15 ; Similar to TXM_TRANSMIT_0
599      JB TXM_START_BIT_14, TXM_BYTE_14
600      CLR P3.7
601      SETB TXM_START_BIT_14
602      JMP TXM_TRANSMIT_15
603
604      TXM_BYTE_14:      DJNZ TXM_COUNT_14, TXM_DATA_14
605
606      TXM_STOP_14:      SETB P3.7
607      CLR TXM_IN_PROGRESS_14
608      JMP TXM_EXIT
609
610      TXM_DATA_14:      MOV A, TXM_REG_14
611      RRC A
612      RRC P3.7, C
613      MOV TXM_REG_14, A
614      JMP TXM_EXIT
615
616      ;
617      ;
618      ;
619      TXM_TRANSMIT_15:      JNB TXM_IN_PROGRESS_15, TXM_TRANSMIT_16 ; Similar to TXM_TRANSMIT_0
620      JB TXM_START_BIT_15, TXM_BYTE_15
621      CLR P3.7
622      SETB TXM_START_BIT_15
623      JMP TXM_TRANSMIT_16
624
625      TXM_BYTE_15:      DJNZ TXM_COUNT_15, TXM_DATA_15
626
627      TXM_STOP_15:      SETB P3.7
628      CLR TXM_IN_PROGRESS_15
629      JMP TXM_EXIT
630
631      TXM_DATA_15:      MOV A, TXM_REG_15
632      RRC A
633      RRC P3.7, C
634      MOV TXM_REG_15, A
635      JMP TXM_EXIT
636
637      ;
6
```

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MCS-51 MACRO ASSEMBLER

SWPORT

```

LUC OBJ      LINE      SOURCE
0139 C3      364      CLR C          ; Update compare value with
013A 742C      365      MOV A, CCAP3L    ; full bit line 22CH
013B 752D      366      ADD A, CCAP3L
013C 752D      367      MOV CCAP3H, A
013D 752D      368      MOV A, CCAP3H
013E 752D      369      MOV CCAP3H, A
013F 752D      370      MOV CCAP3H, A
0140 752D      371      POP PSW
0141 0000      372      POP ACC
0142 0000      373      RETI
0143 0000      374      ;
0144 32        375      ;
0145 0000      376      ;
0146 0000      377      ;
0147 0000      378      ;
0148 0000      379      ;
0149 0000      380      ; When a byte is received on the full-duplex serial port, it is then
014A 0000      381      ; transmitted back to a "dummy" terminal. This terminal checks that
014B 0000      382      ; the byte it transmitted to the PCA is the same value it receives back.
014C 0000      383      ;
014D 0000      384      ; SERIAL PORT:
014E 0000      385      PUSH ACC
014F 30980B      386      JNB RI, TXM          ; Check whether RI or TI
0150 6599      387      CLR RI, SBUF          ; caused the interrupt
0151 6599      388      MOV A, SBUF
0152 6599      389      MOV SBUF, A
0153 0000      390      POP PSW
0154 0000      391      POP ACC
0155 32        392      RETI
0156 0000      393      ;
0157 0000      394      ; TXM:
0158 0000      395      CLR RI
0159 0000      396      POP PSW
0160 0000      397      POP ACC
0161 0000      398      RETI
0162 32        399      ;
0163 32        400      END

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